

COVER SHEET	1
BLOCK DIAGRAM	2
CLOCK MAP	3
POWER MAP	4
GPIO MAP	5
Intel Diamondville-CPU	6-7
VRM Single Phase	8
Intel Lakeport -GMCH	9-12
DDR II SO-DIMM	13-14
Mini PCIE Slot	15
CLK - Realtek RTM876-665	16
VGA CONNECTOR	17
CH7307 & DVI CONNECTOR	18
LAN 8111C	19
ICH7	20-22
TPM LPC Debug port	23
USB CONNECTORS	24
Front Panel&Card	25
+19V DC-IN	26
ACPI Controller	27
HD AUDIO CODEC(ALC 888)	28
SATA & SIO F71882 & FAN CONTROL	29
Auto BOM manual	30
PWOK MAP	31
History	32

# MS-7445

## CPU:

Intel Atom

## System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

## On Board Chipset:

SIO -- Fintek 71882

BIOS -- SPI

HD AUDIO CODEC(ALC888)

LAN -- Realtek RTL8111C

Clock Generator -- Real RTM876-665

DVI -- CH7307

## Main Memory:


DDR II SO-DIMM x 1 (Max 2GB)

## Expansion Slots:

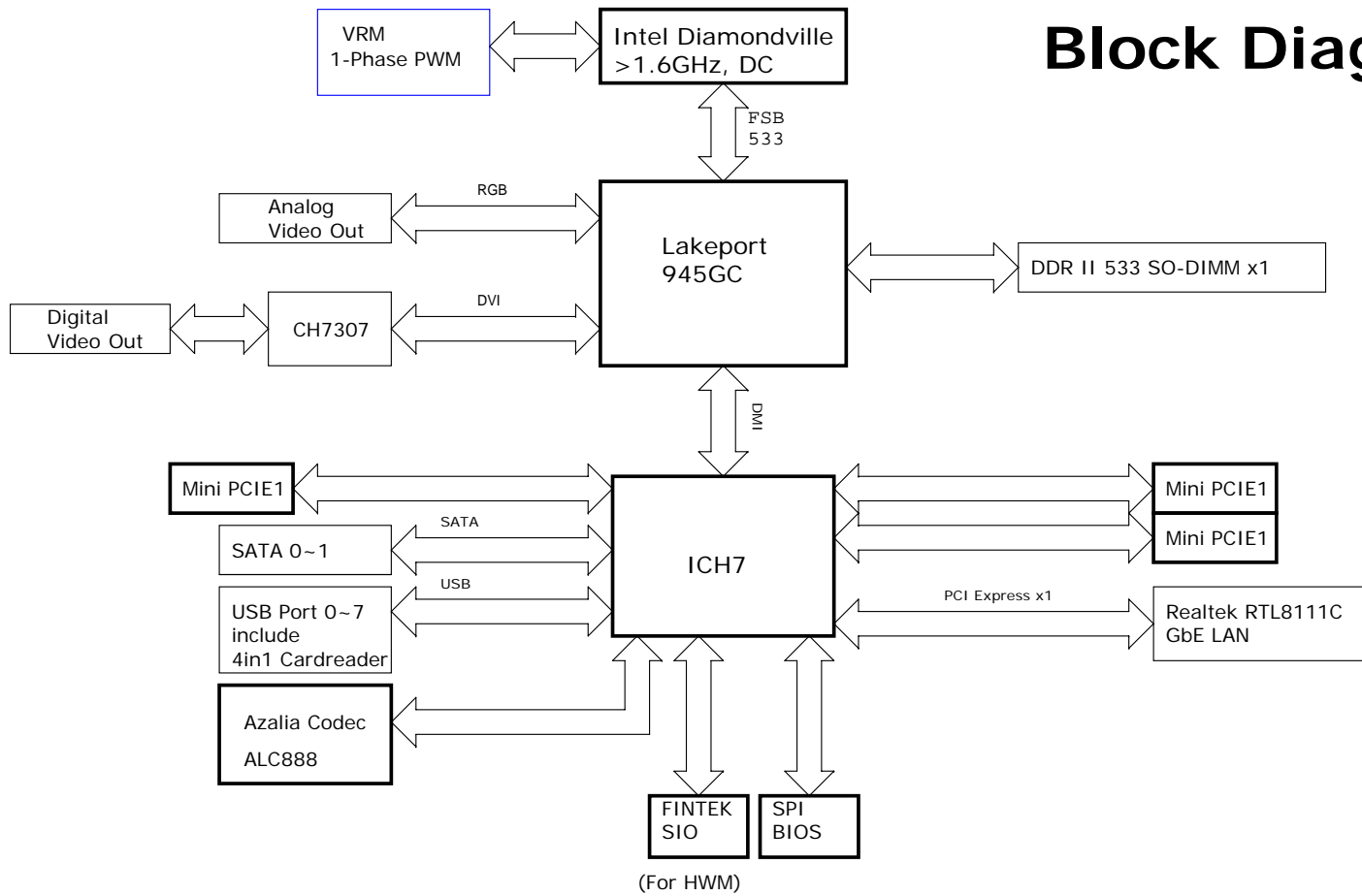
Internal Mini PCIE x2

## Intersil PWM:

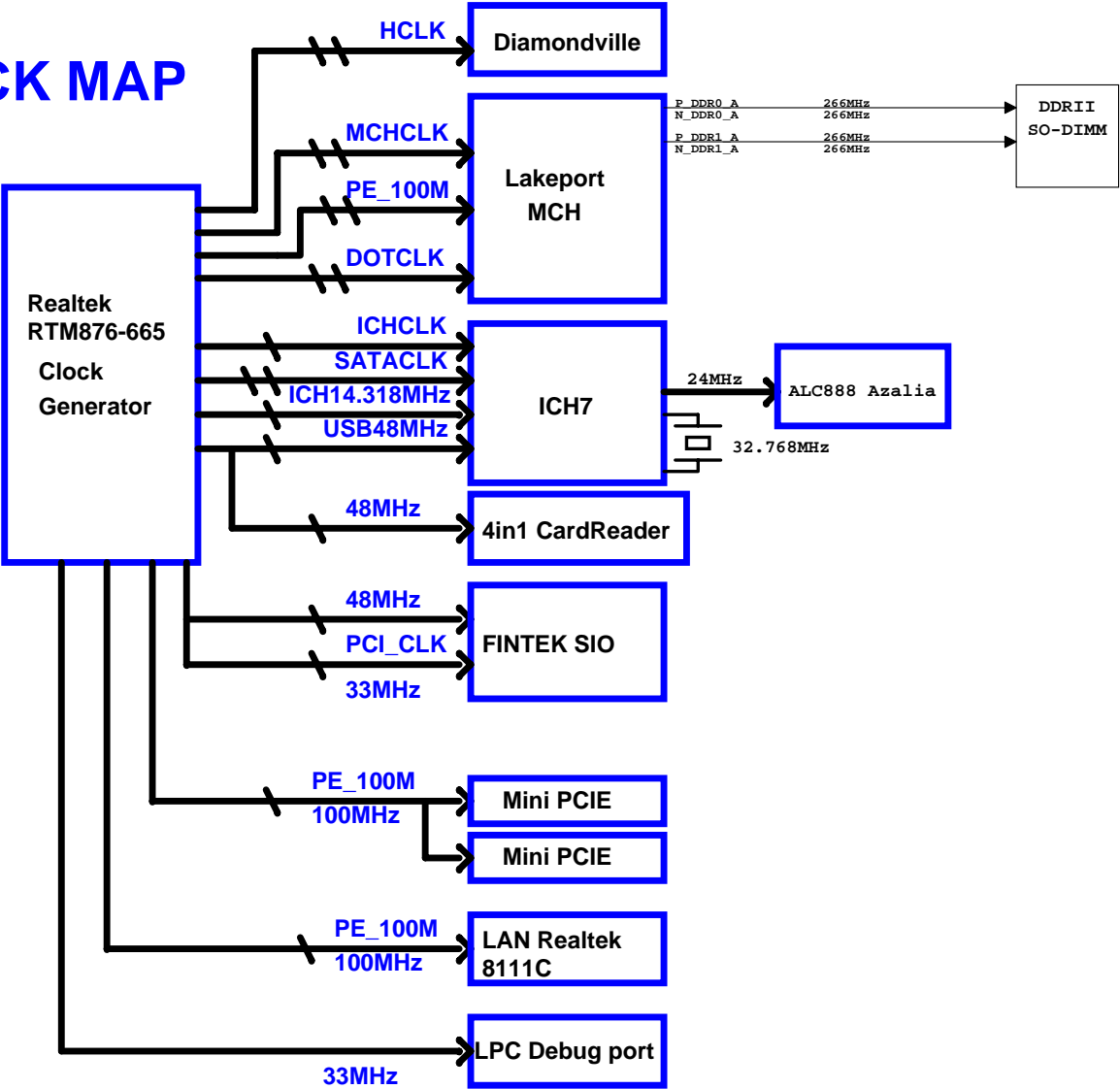
Controller: 6314

 <b>MICRO-STAR INT'L CO., LTD.</b>	
Title: COVER SHEET	
Size: Document Number	Rev: 0A
MS-7445	
Date: Friday, December 26, 2008	Sheet 1 of 32

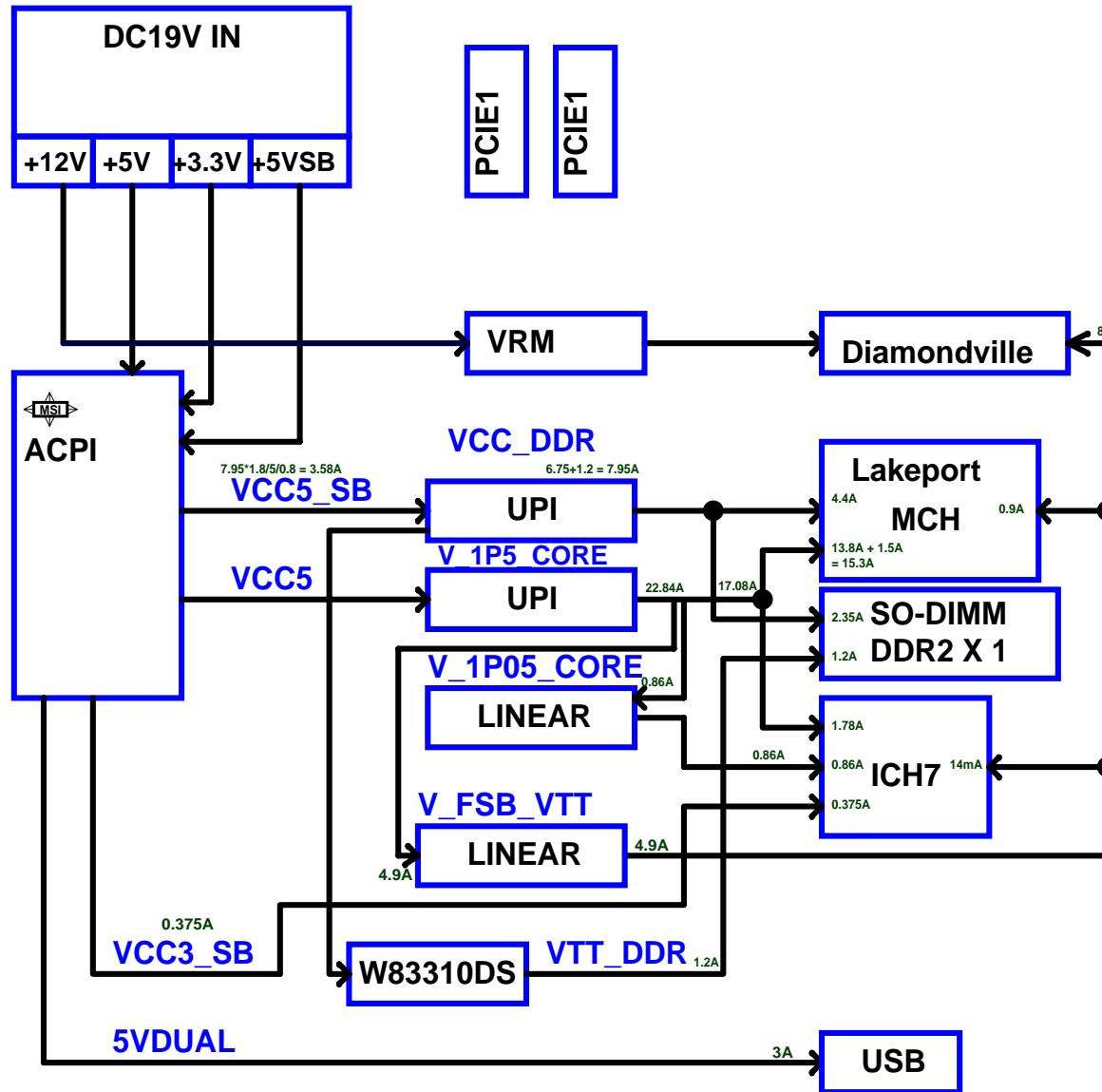
# Block Diagram



# CLOCK MAP



# POWER MAP



ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]		AC21	I/O	Vcc3p3	N	Y	3.3	Input	
GPIO[7]	OVT#	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	WLAN2_PWRON	A20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA1GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	NC
GPIO[25]	unmuxed	D20	I/O	VccSus3p3	Y	N	3.3	1	pull high VCC3 SB
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:  
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3\_3 if unused.  
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3\_3 if unused.

SIGNAL	DEVICE
MiniPCleRST#	MINI PCIE SLOT
TPMRST#	TPM & SIO
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
PCIRST_DVI#	CH7307C
H_CPURST#	CPU
FWHRST#	LPT Debug port
MCHRST#	MCH

SMBCLK, SMBDATA	DDR2, PCIEX1, CLKGEN, ICH7
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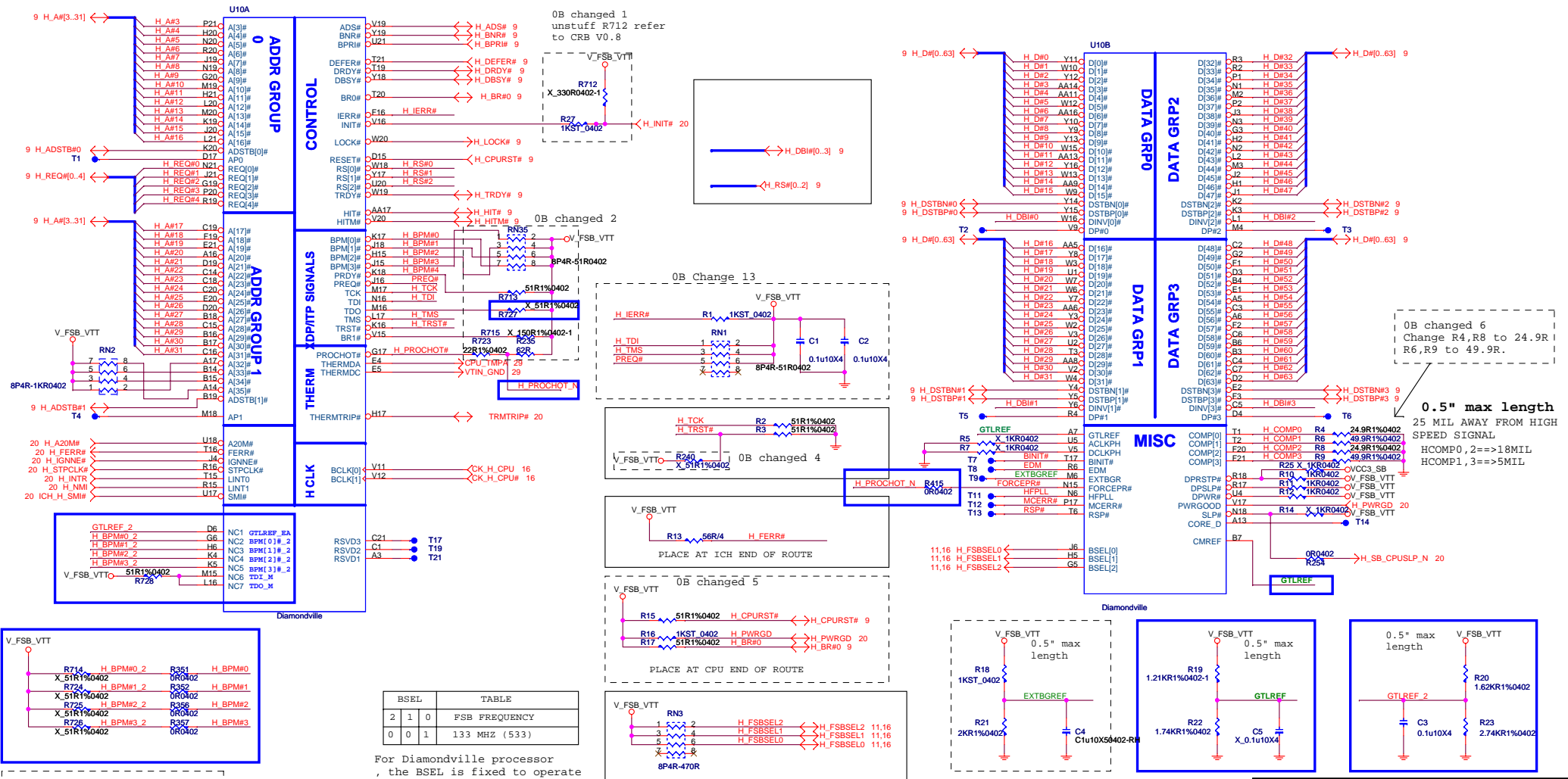
DDRII DIMM Config.

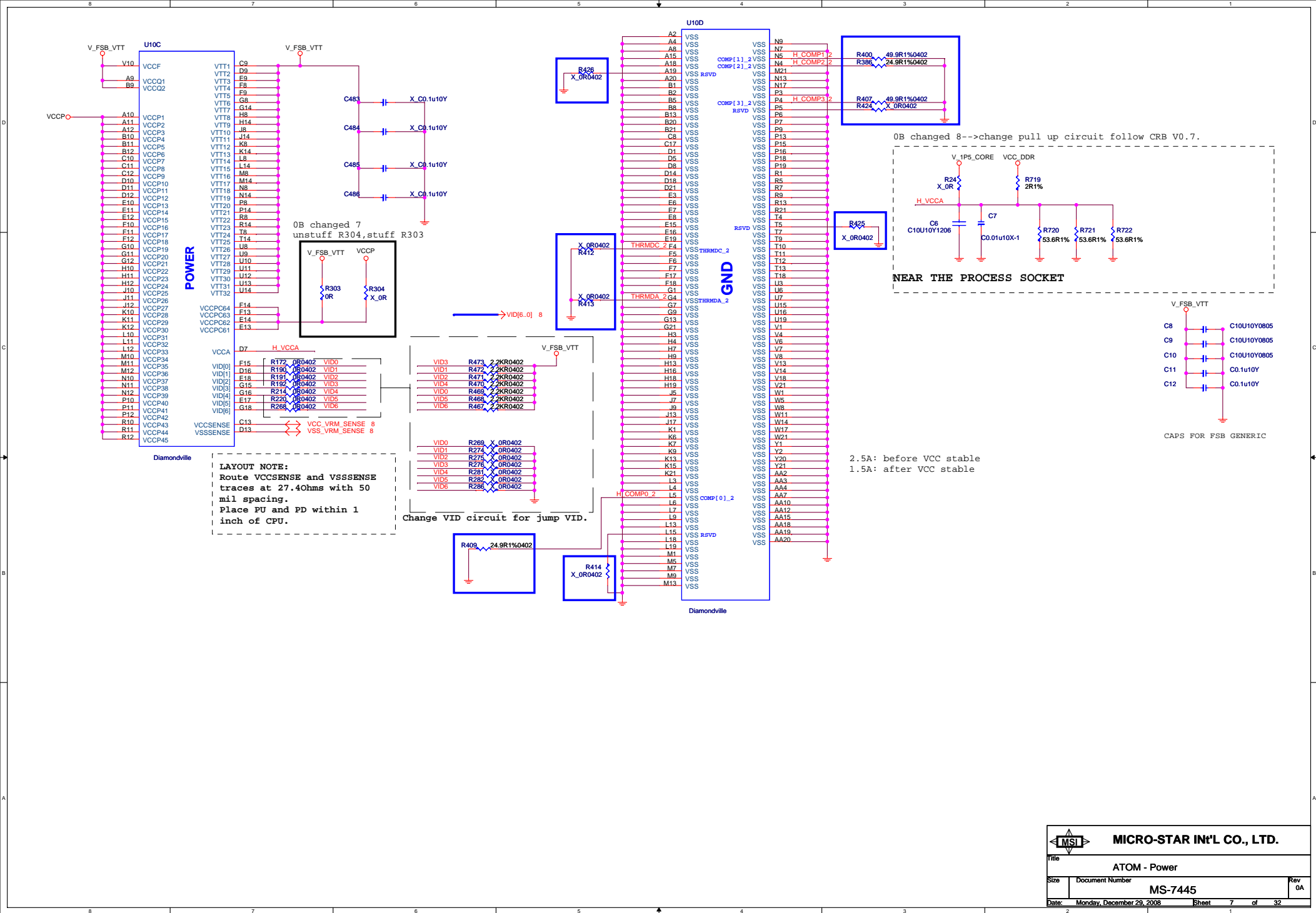
DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

JUMPER SETTING

<b>JBAT1</b>	(1-2) NORMAL	(2-3) CLEAR
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# CPU SIGNAL BLOCK









13.14 SCS\_A# [0..1] <->

13.14 RAS\_A# <->  
13.14 CAS\_A# <->  
13.14 WE\_A# <->

13.14 MAA\_A# [0..13] <->

13.14 ODT\_A# [0..1] <->

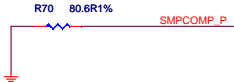
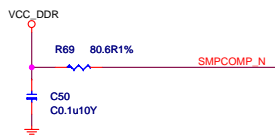
13.14 SBS\_A# [0..2] <->

13 DQS\_A0 <->  
13 DQS\_A#0 <->  
13 DQS\_A1 <->  
13 DQS\_A#1 <->  
13 DQS\_A2 <->  
13 DQS\_A#2 <->  
13 DQS\_A3 <->  
13 DQS\_A#3 <->  
13 DQS\_A4 <->  
13 DQS\_A#4 <->  
13 DQS\_A5 <->  
13 DQS\_A#5 <->  
13 DQS\_A6 <->  
13 DQS\_A#6 <->  
13 DQS\_A7 <->  
13 DQS\_A#7 <->

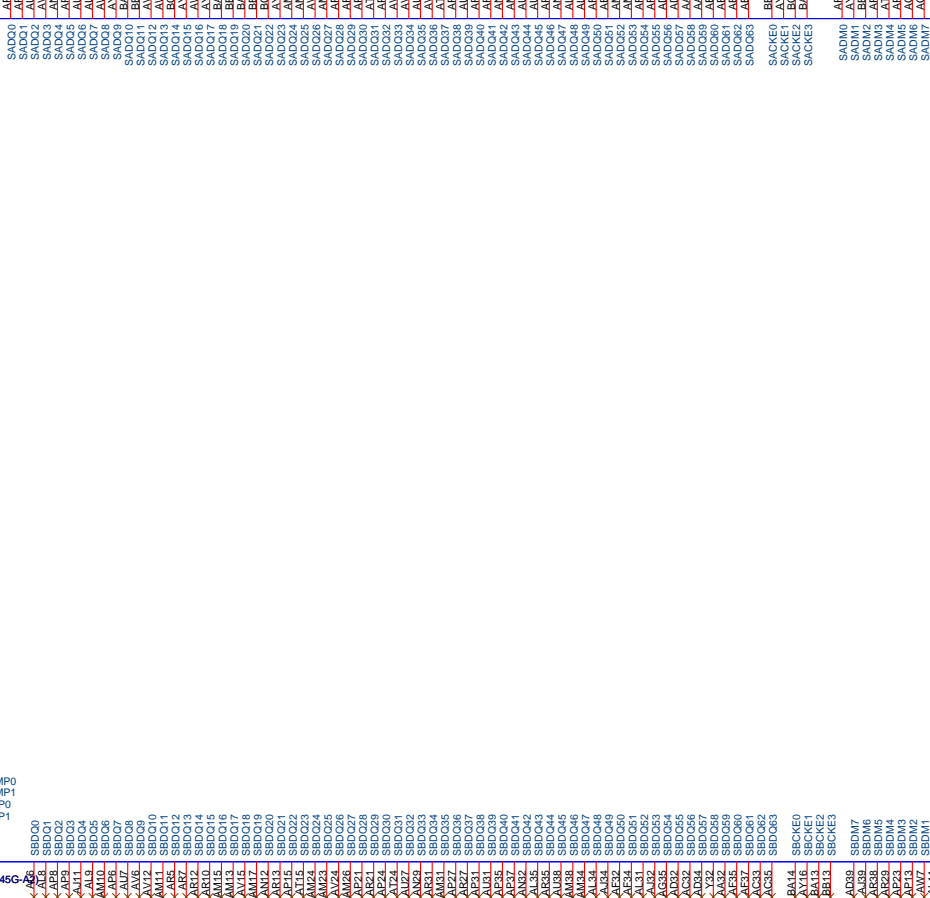
13 P\_DDR0\_A <->  
13 N\_DDR0\_A <->  
13 P\_DDR1\_A <->  
13 N\_DDR1\_A <->

SMPCOMP\_N <->  
SMPCOMP\_P <->

Rule:  
SMPCOMP\_N 12mils  
SMPCOMP\_P 12mils



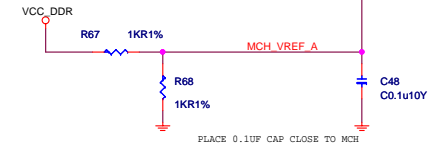
13.14 DATA\_A# [0..63] <->  
13.14 SCKE\_A# [0..1] <->  
13 DOM\_A# [0..7] <->



SBCS0# <->  
SBCS1# <->  
SBCS2# <->  
SBCS3# <->  
SBAS# <->  
SBAS# <->  
SBWE# <->  
SBMA0 <->  
SBMA1 <->  
SBMA2 <->  
SBMA3 <->  
SBMA4 <->  
SBMA5 <->  
SBMA6 <->  
SBMA7 <->  
SBMA8 <->  
SBMA9 <->  
SBMA10 <->  
SBMA11 <->  
SBMA12 <->  
SBMA13 <->  
SBODT0 <->  
SBODT1 <->  
SBODT2 <->  
SBODT3 <->  
SBA0 <->  
SBA1 <->  
SBA2 <->  
SBDQS0 <->  
SBDQS# <->  
SBDQS1 <->  
SBDQS# <->  
SBDQS2 <->  
SBDQS# <->  
SBDQS3 <->  
SBDQS# <->  
SBDQS4 <->  
SBDQS# <->  
SBDQS5 <->  
SBDQS# <->  
SBDQS6 <->  
SBDQS# <->  
SBDQS7 <->  
SBDQS# <->  
SBCLK0 <->  
SBCLK# <->  
SBCLK1 <->  
SBCLK# <->  
SBCLK2 <->  
SBCLK# <->  
SBCLK3 <->  
SBCLK# <->  
SBCLK4 <->  
SBCLK# <->  
SBCLK5 <->  
SBCLK# <->

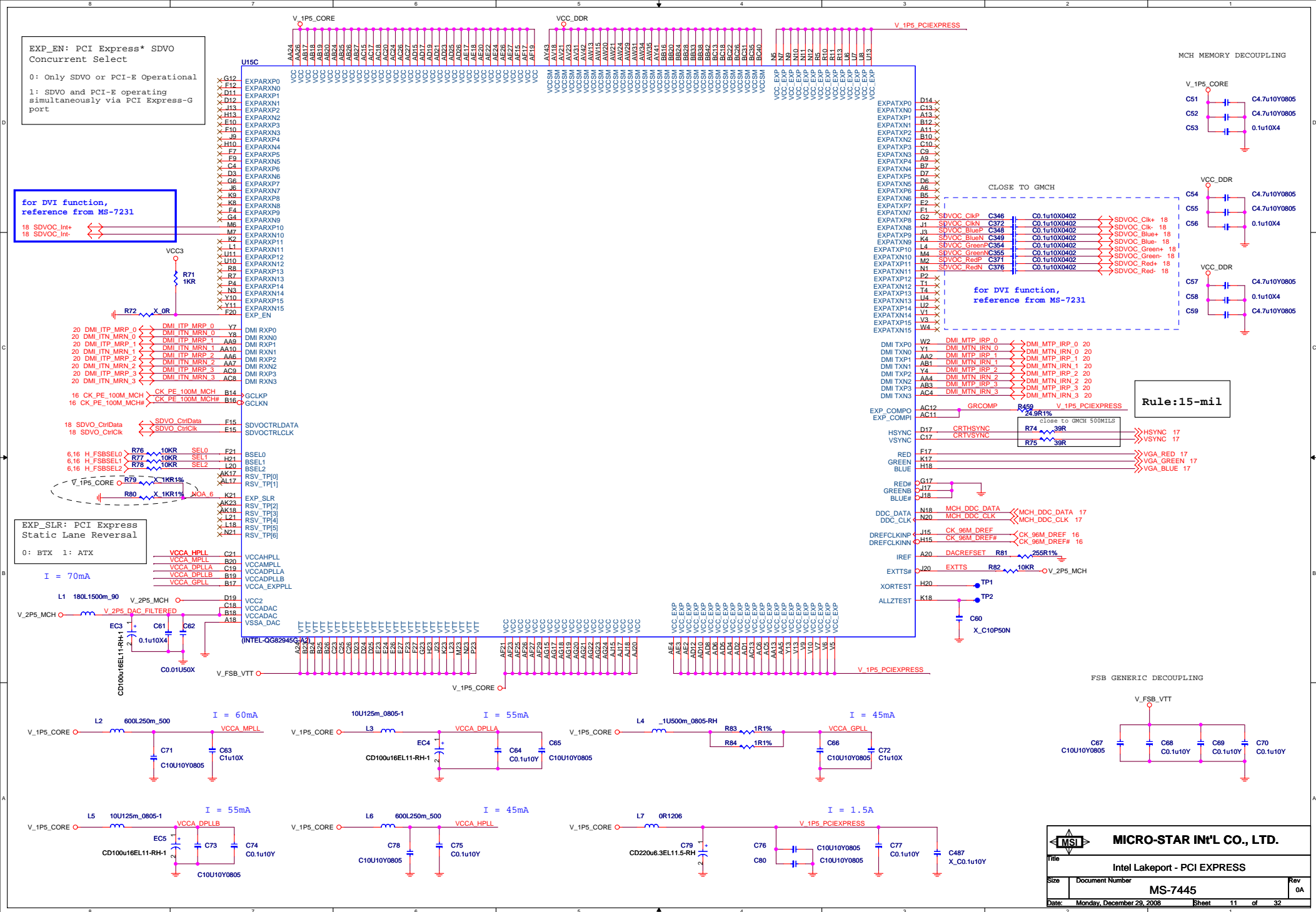


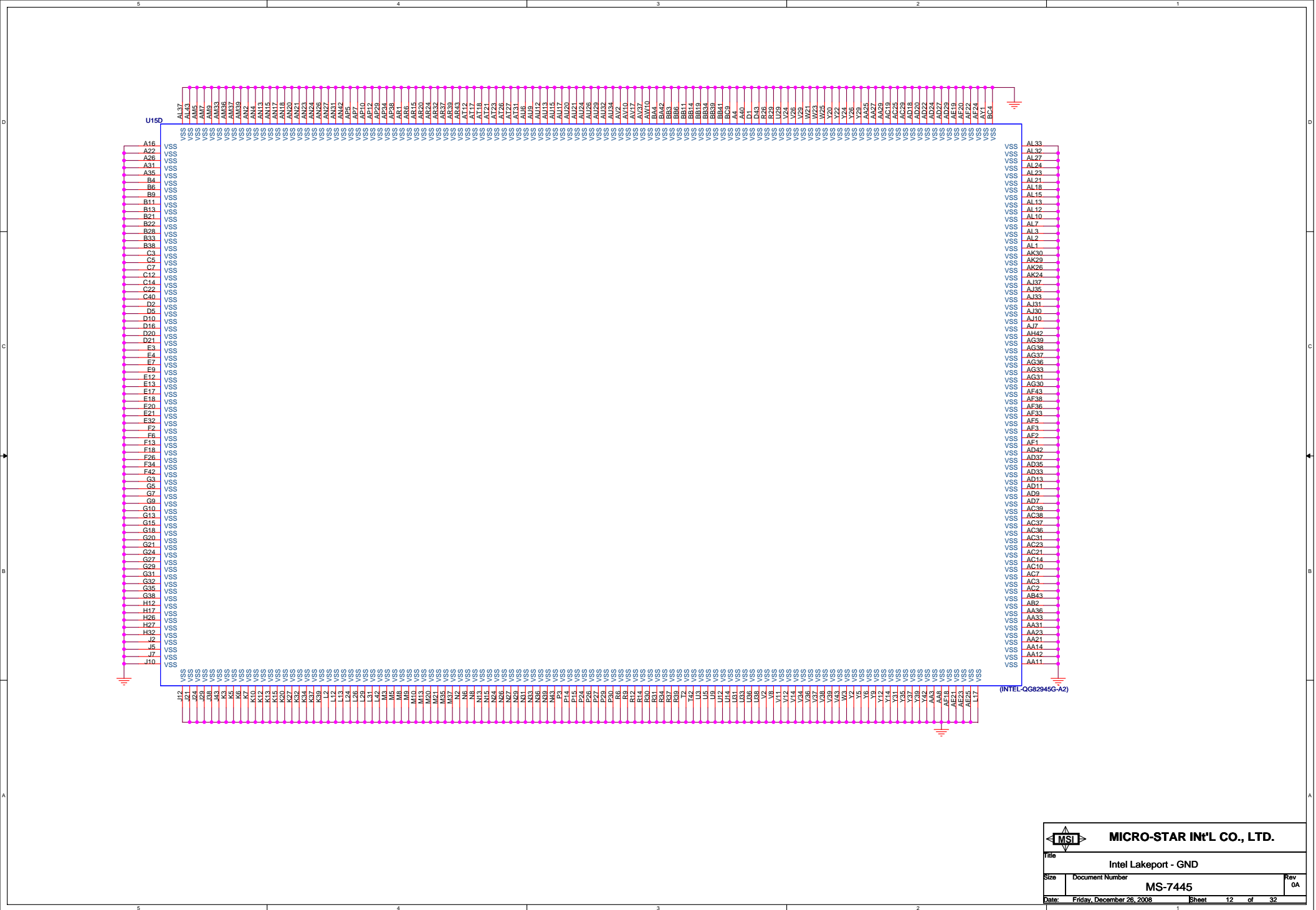
PLACE 0.1UF CAP CLOSE TO MCH



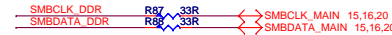
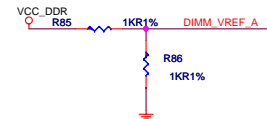
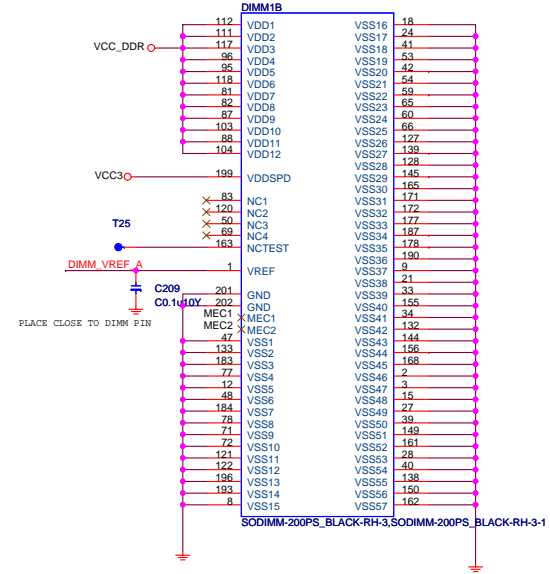
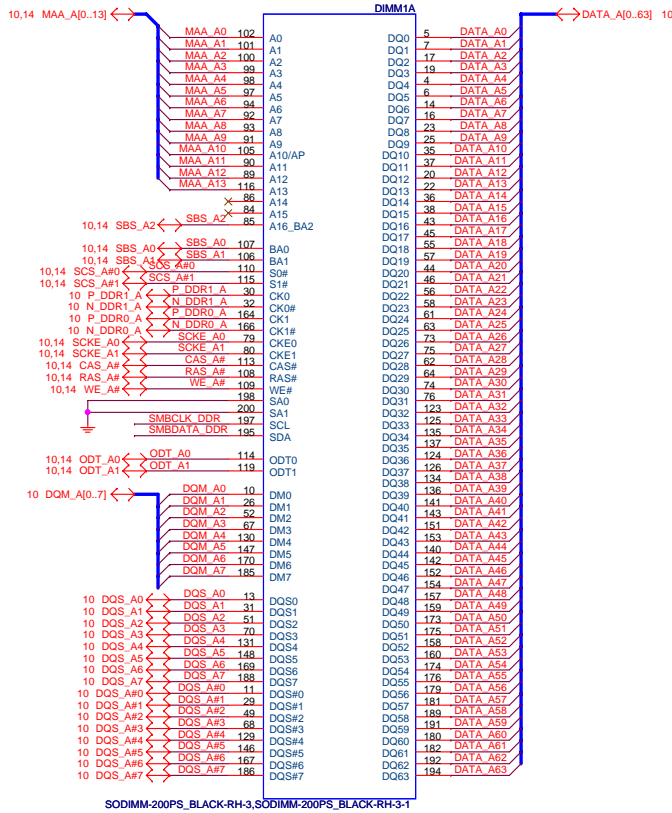
PLACE 0.1UF CAP CLOSE TO MCH

MSI		
Intel Lakeport - Memory		
Size	Document Number	Rev
	MS-7445	0A
Date:	Monday, December 29, 2008	Sheet 10 of 32





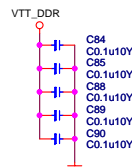
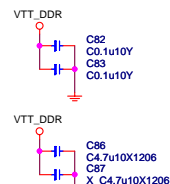
# DDR2 SO-DIMM



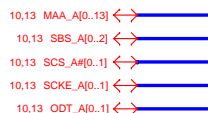
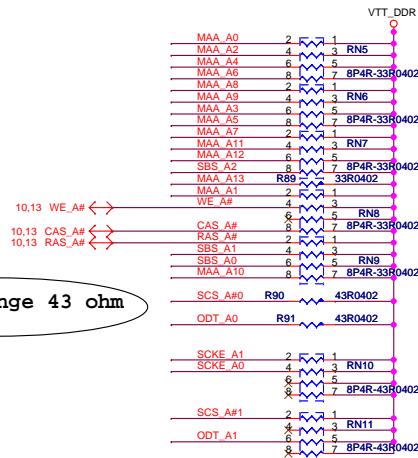
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Title		DDR II SO-DIMM	
Document Number		MS-7445	
Date	Monday, December 29, 2008	Sheet	13 of 32

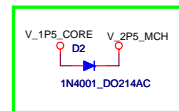
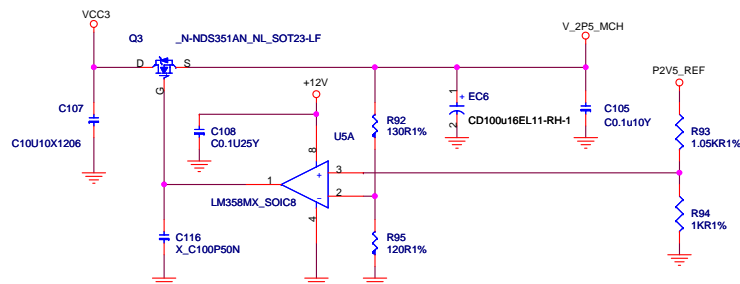
# CHANNEL A V\_SM\_VTT DECOUPLING CAPS

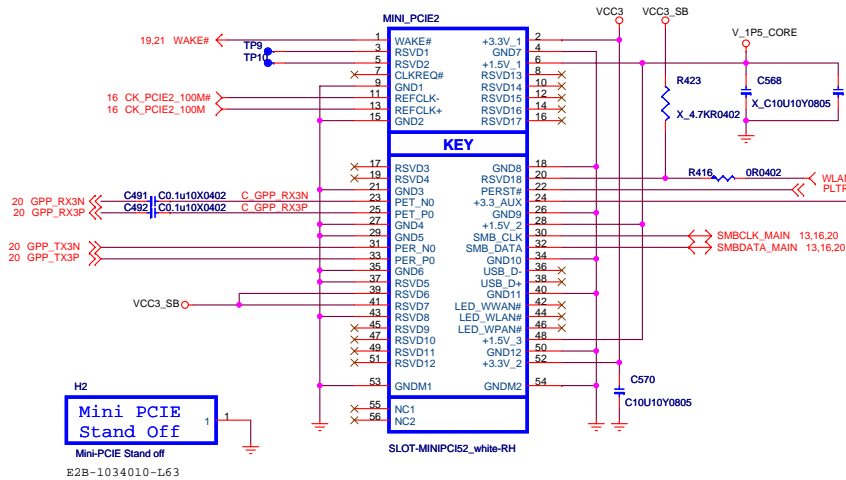
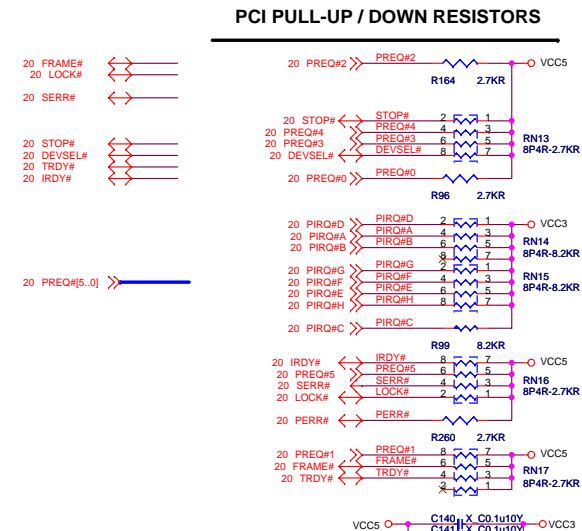
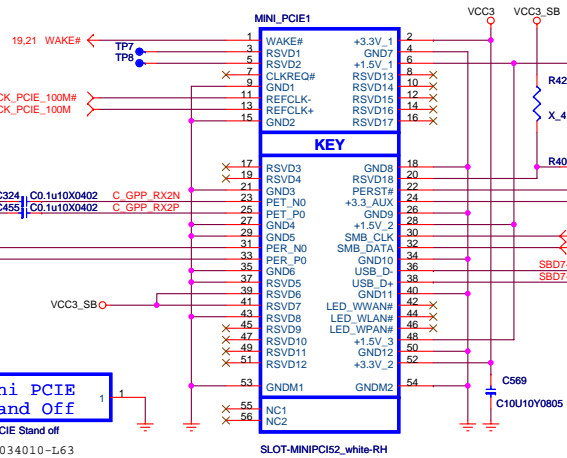


SCS\_A#0 change 43 ohm

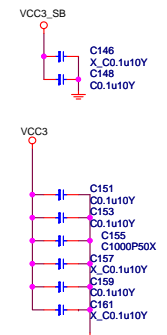


## Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC

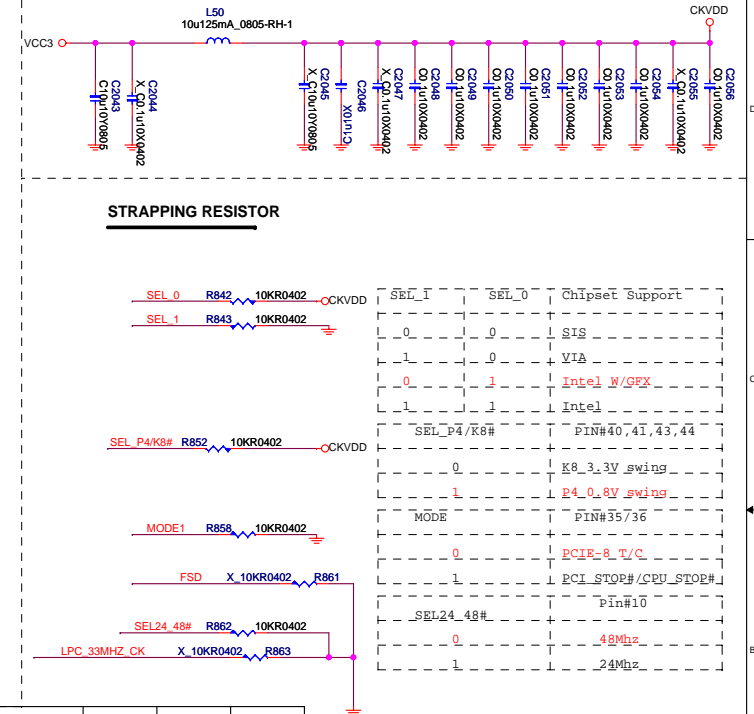
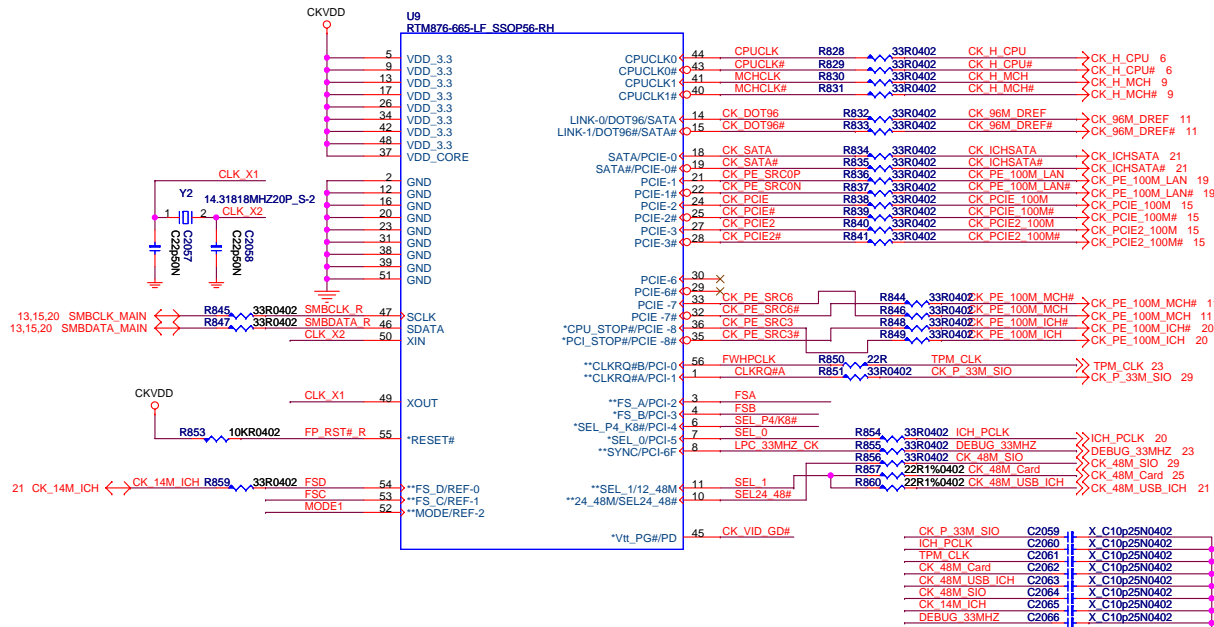




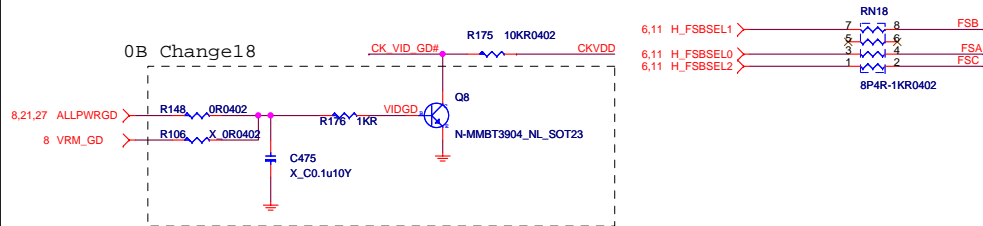
## DECOUPLING CAPACITORS



## Clock Generator - RTM876-665



## Clock Generator VTT Power Down Block



(FSLC, FSLB, FSLA)	CPU MHz	PCIEX MHz	PCI MHz
( 0 , 0 , 0 )	266.66	100.00	33.33
( 0 , 0 , 1 )	133.33	100.00	33.33
( 0 , 1 , 0 )	200.00	100.00	33.33
( 0 , 1 , 1 )	166.66	100.00	33.33
( 1 , 0 , 0 )	333.33	100.00	33.33
( 1 , 0 , 1 )	100.00	100.00	33.33
( 1 , 1 , 0 )	400.00	100.00	33.33



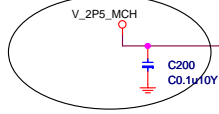
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MS-7445

Size	Document Description	Rev
Custom	CLK-RTM876-665	0A
Date: Monday, December 29, 2008	Sheet 16 of 32	

# Video Connector

Power 20 mils



After 150 ohm

5 mils

before 150 ohm

12 mils

7 mils

Avoid leakage from Monitor

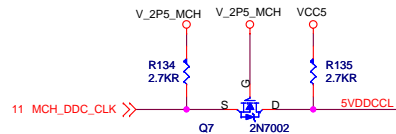
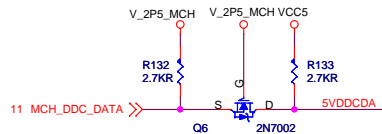
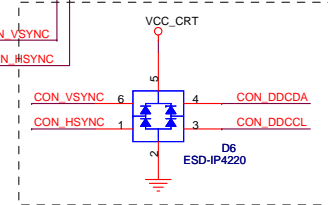
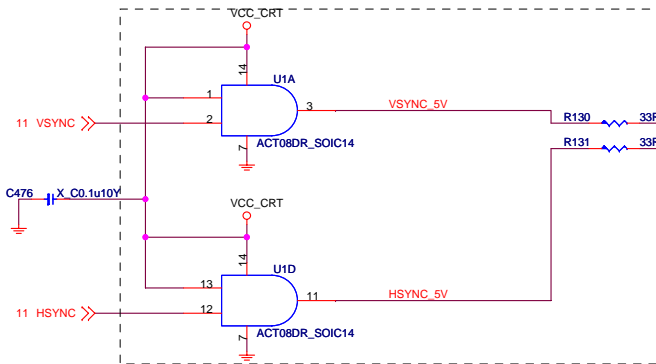
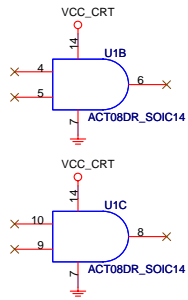


PLACE CLOSE TO MCH,  
WITHIN 500 MIL OF  
PIN

PLACE CLOSE TO VGA CONNECTOR

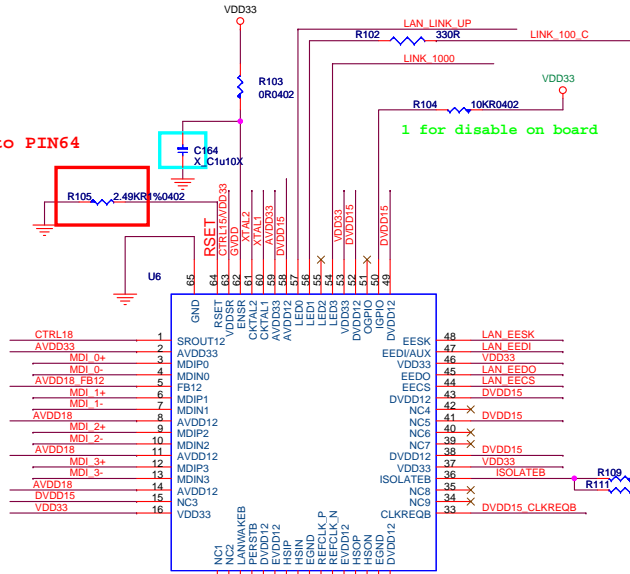
CONN-D-SUB\_blue-3.18mm

PLACE CLOSE TO VGA CONNECTOR





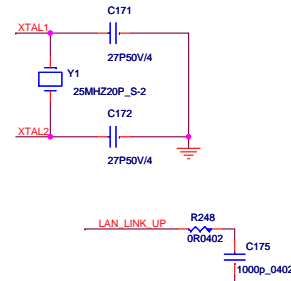
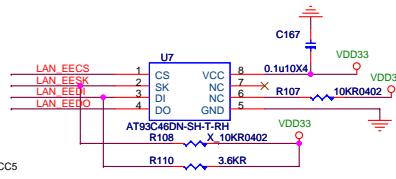
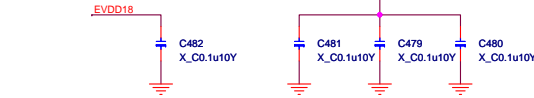
layout close to PIN64



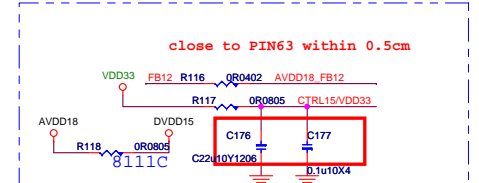
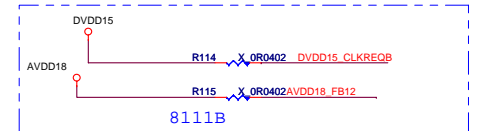
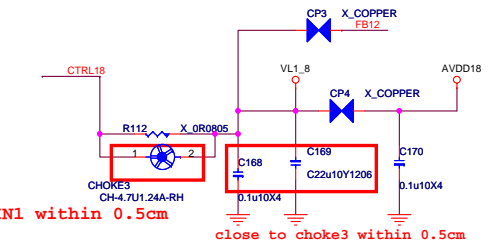
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q9	Q10
RTL8111B	Need	Need
RTL8111C	N/A	N/A



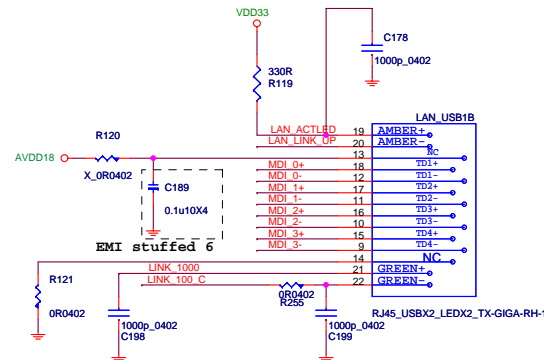
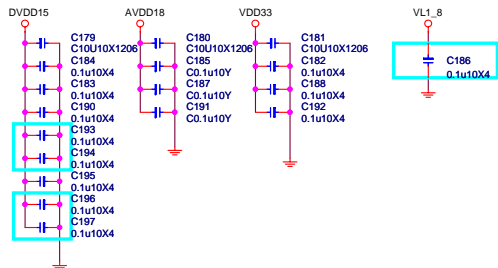
close to PIN1 within 0.5cm

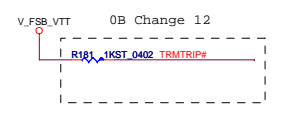
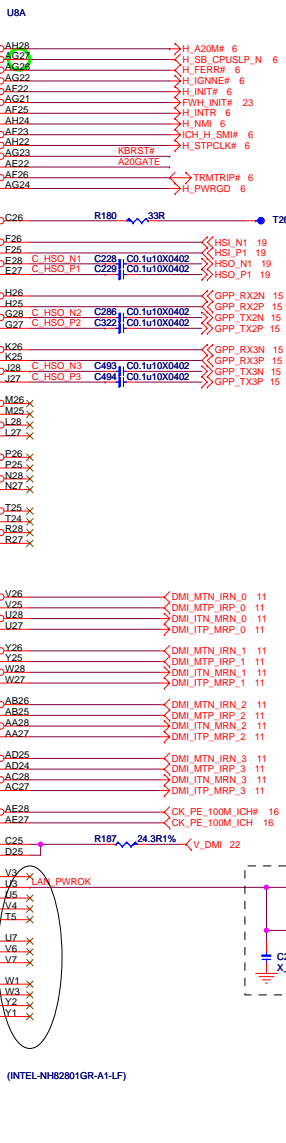
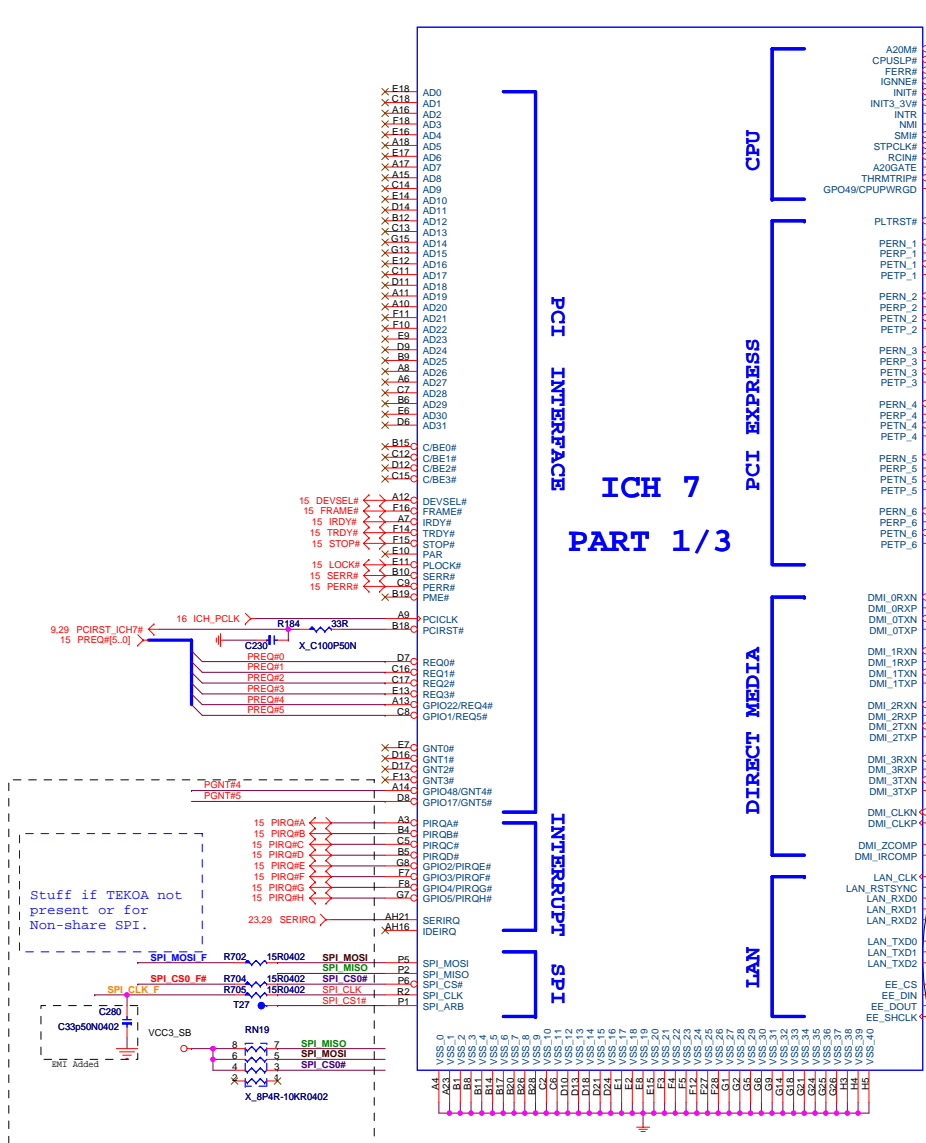


Power consumption	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

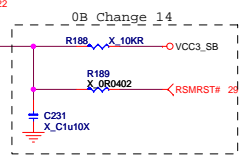
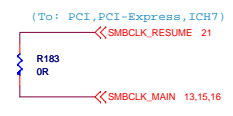
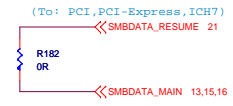
  

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0061-S42
N58-22F0061-F02	N58-22F0061-F02
Link Active 1000	Link Active 1000
Blinking 1000	Blinking 1000
Orange 100	Orange 100
Green 10	Green 10
None 10	None 10
Yellow 19	Yellow 19
Orange 21	Orange 21
Green 22	Green 22

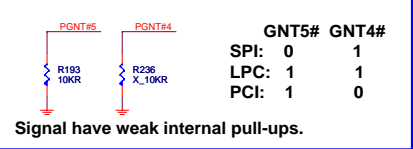




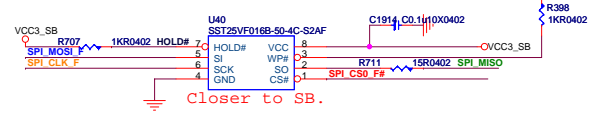
### SM BUS ISOLATION



### Bios Boot Strap

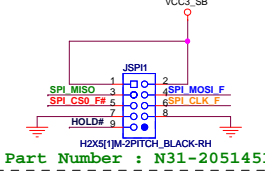


### SPI FLASH (8M)



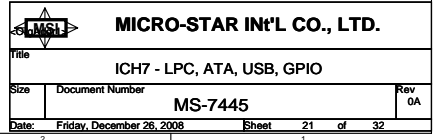
### SPI DEBUG PROT

Place close to SPI ROM

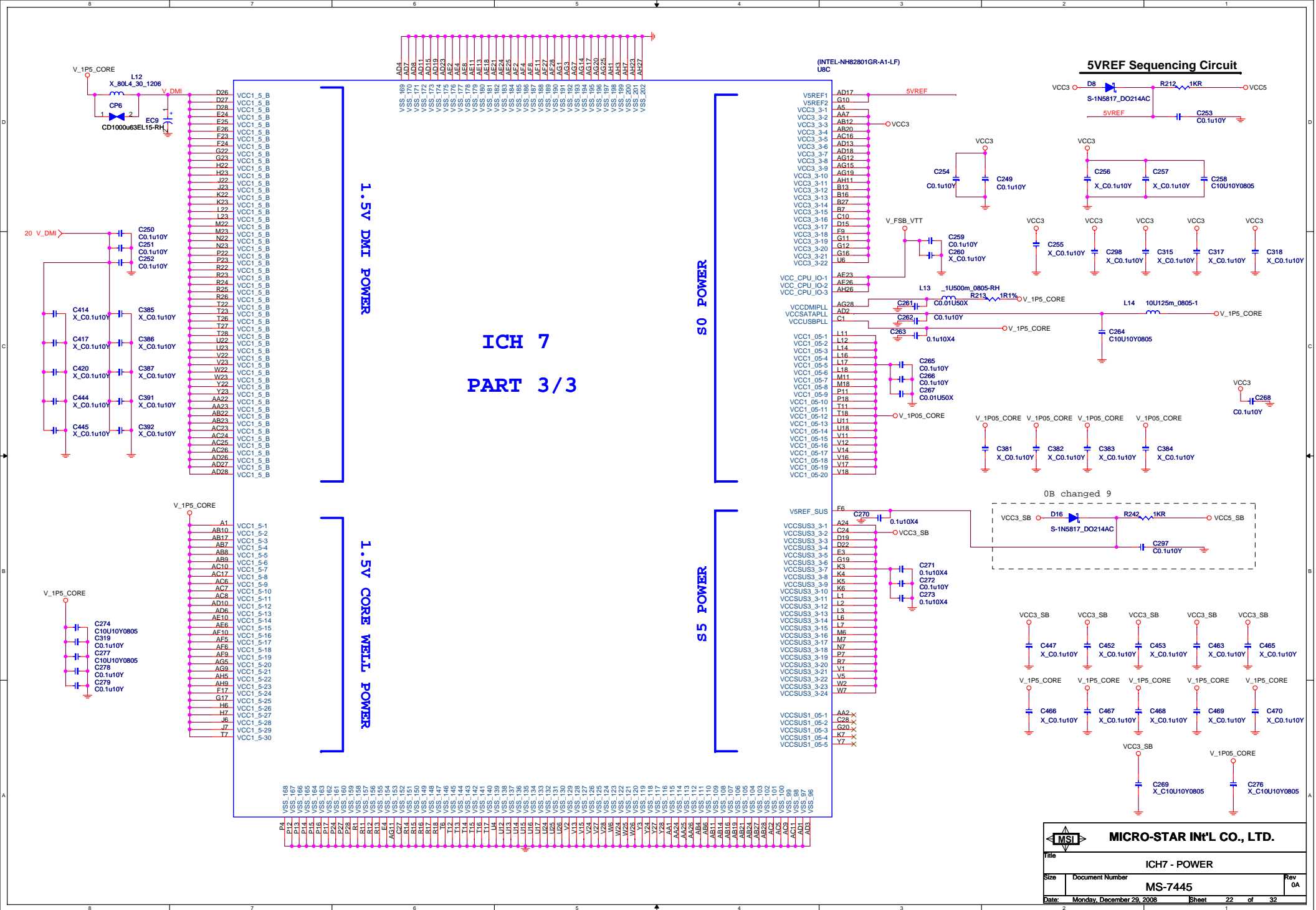




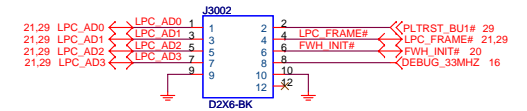
**RTC**



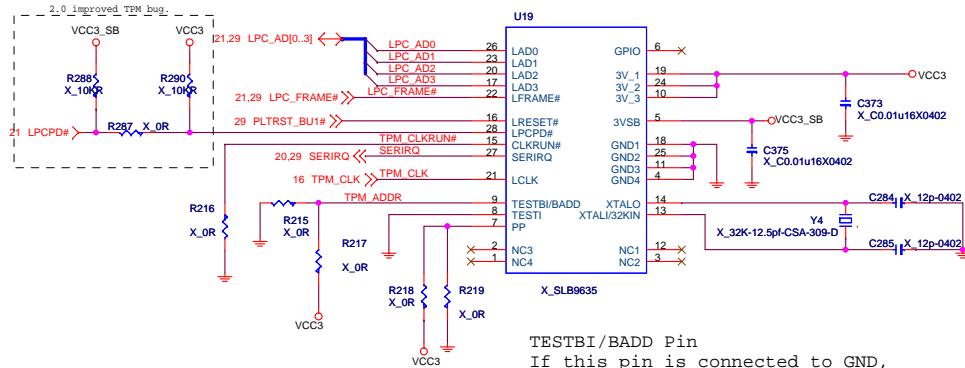
Following are the GPIOs that need to be terminated properly if not used:  
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3\_3 if unused.  
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3\_3 if unused.



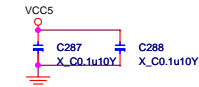
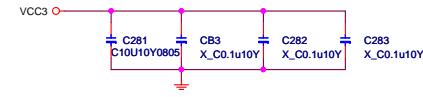
## LPC Debug Port



IO Address: 0x02E



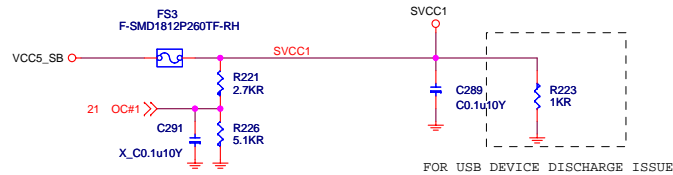
TESTBI/BADD Pin  
If this pin is connected to GND,  
addresses 2EH/2FH are used.  
If it is strapped to VCC,  
addresses 4EH/4FH are used.



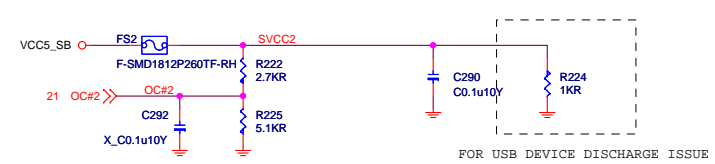
MICRO-STAR IN'L CO., LTD.

Title			FWH		
Size			Document Number		
Date			Rev		
Friday, December 26, 2008			0A		
Sheet			23 of 32		

## POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)

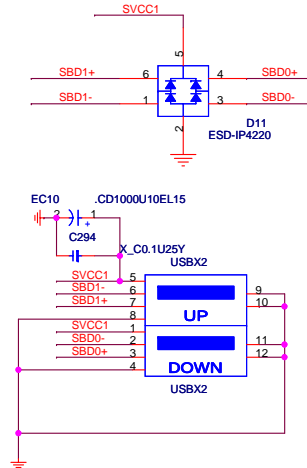
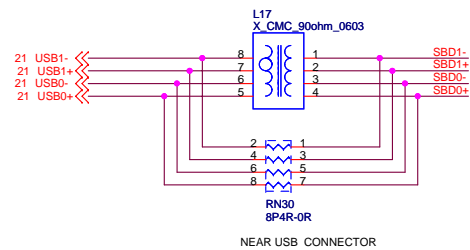


## POWER CIRCUIT FOR USB PORT 4,6,7 (FRONT)



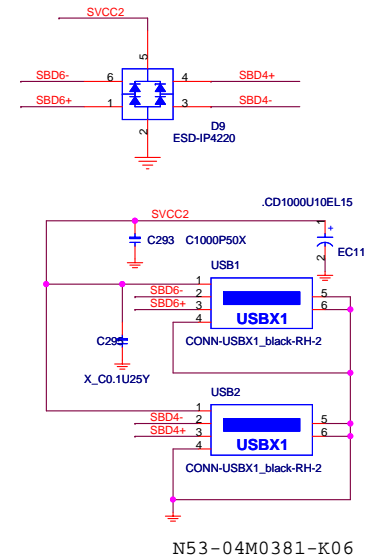
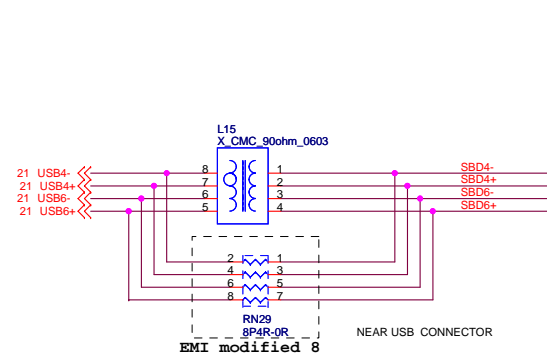
## REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"



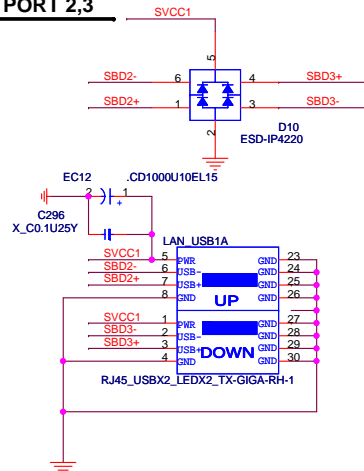
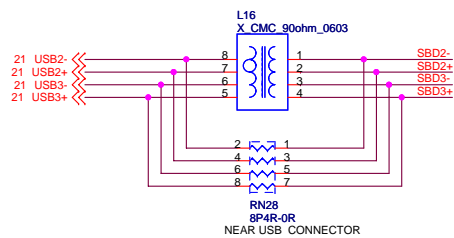
## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"




## REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"



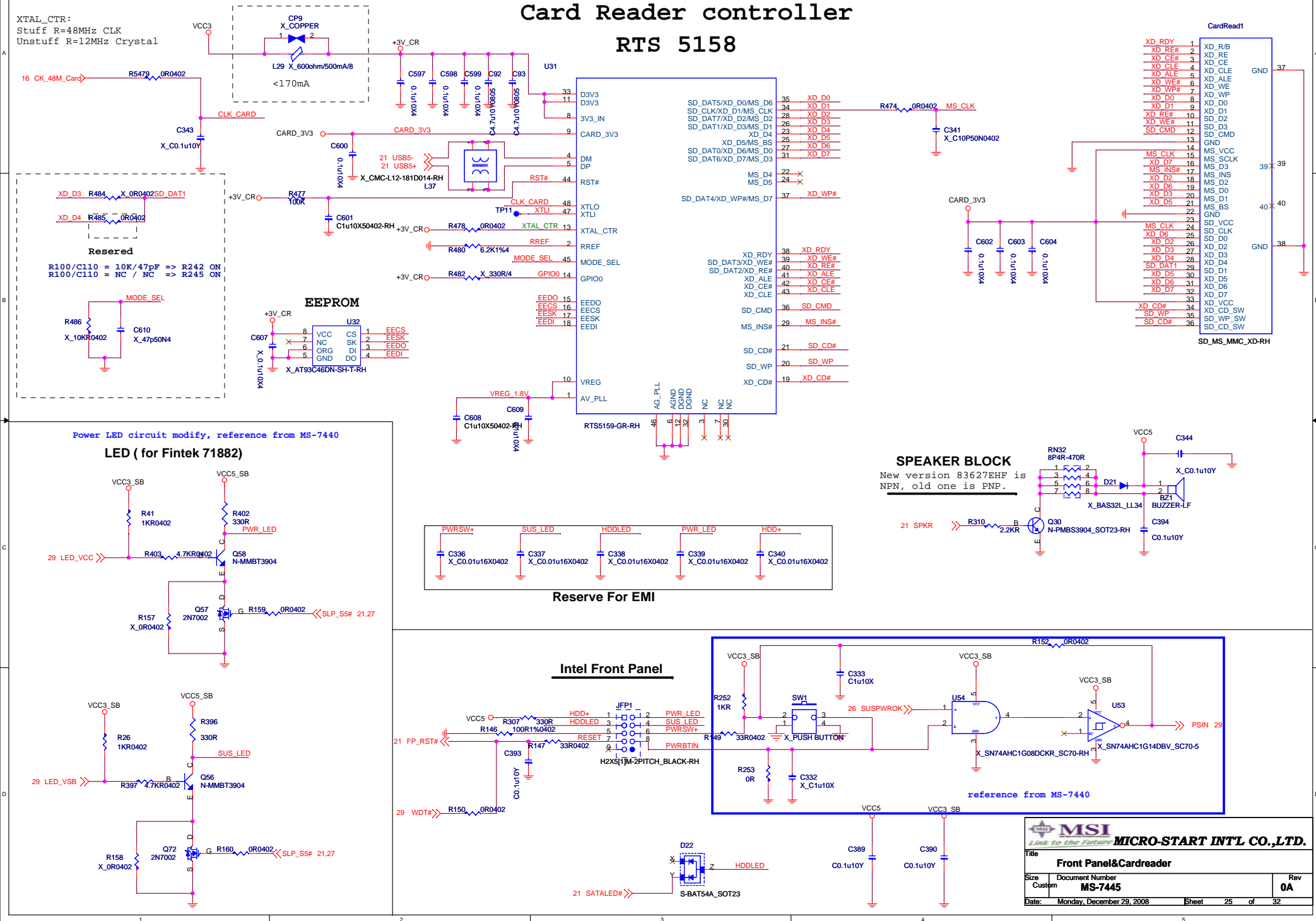
## FRONT PANEL USB CONNECTOR FOR USB PORT 4

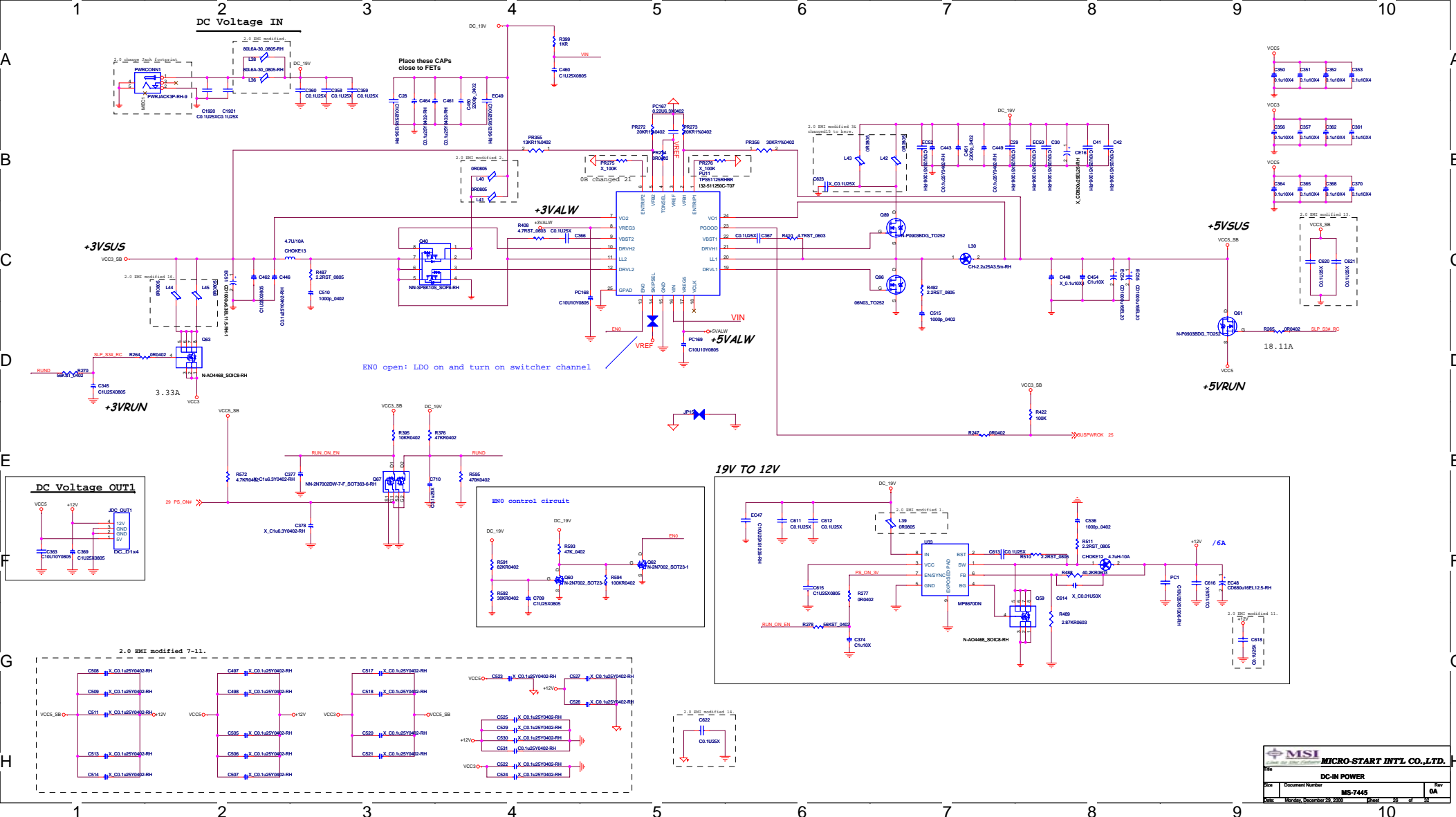
USB Interface  
Diff. Trace width 7.5 mils & 7.5 mils space.  
Diff. & other space 20 mils.  
Length matching: < 150 mils  
Ttrace length 0" to 17"

 <b>MICRO-START INT'L CO.,LTD.</b>		
Title		
USB CONNECTORS		
Size	Document Number	Rev
A3	MS-7445	0A
Date:	Monday, December 29, 2008	Sheet 24 of 32

## Flash Card Socket

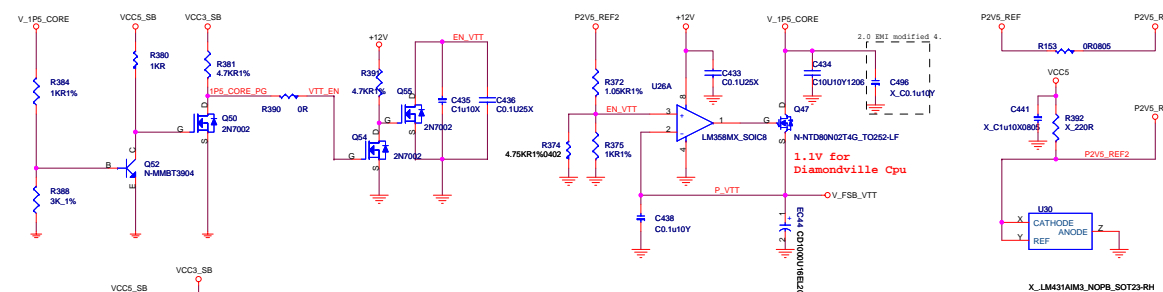
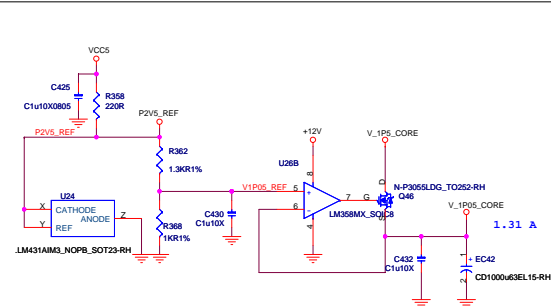
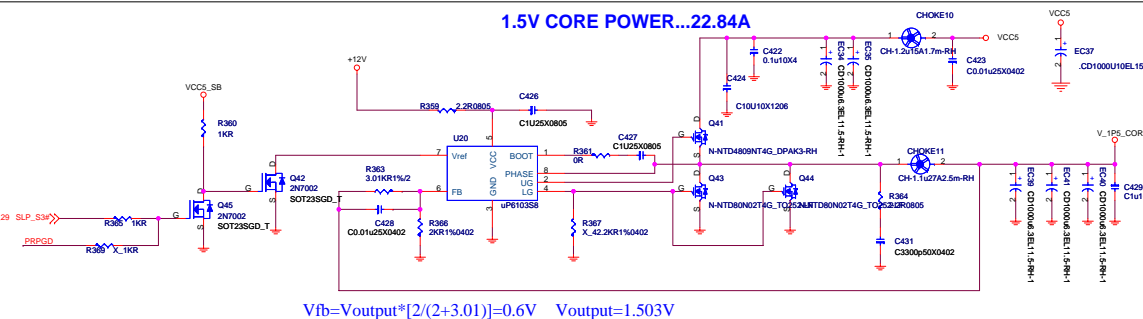
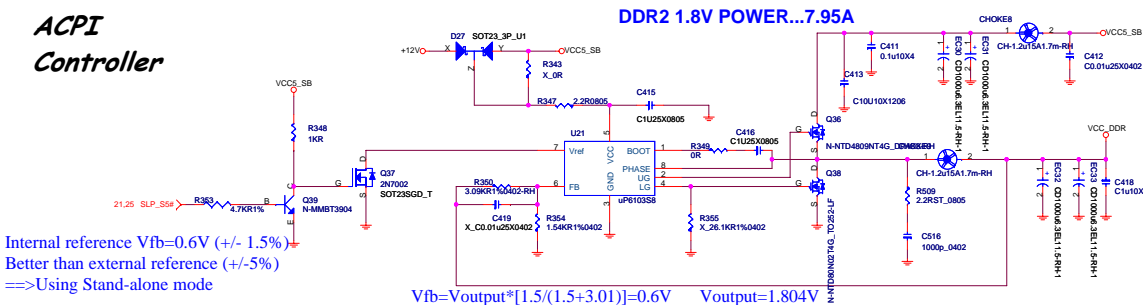
Card Reader controller  
RTS 5158



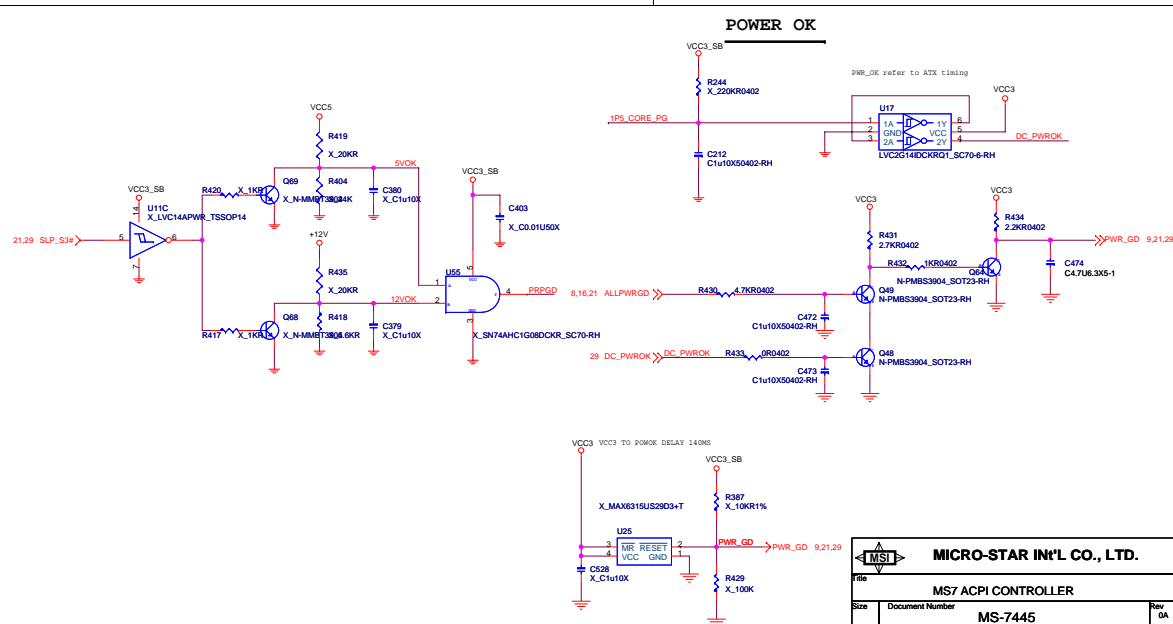
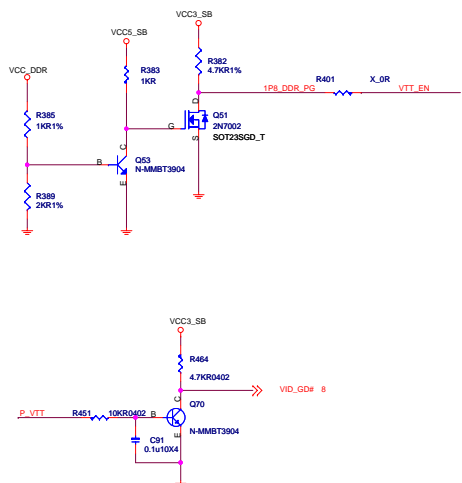
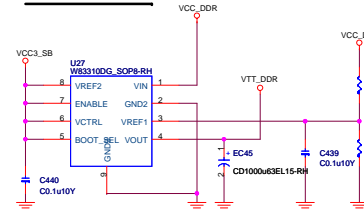


**ACPI  
Controller**

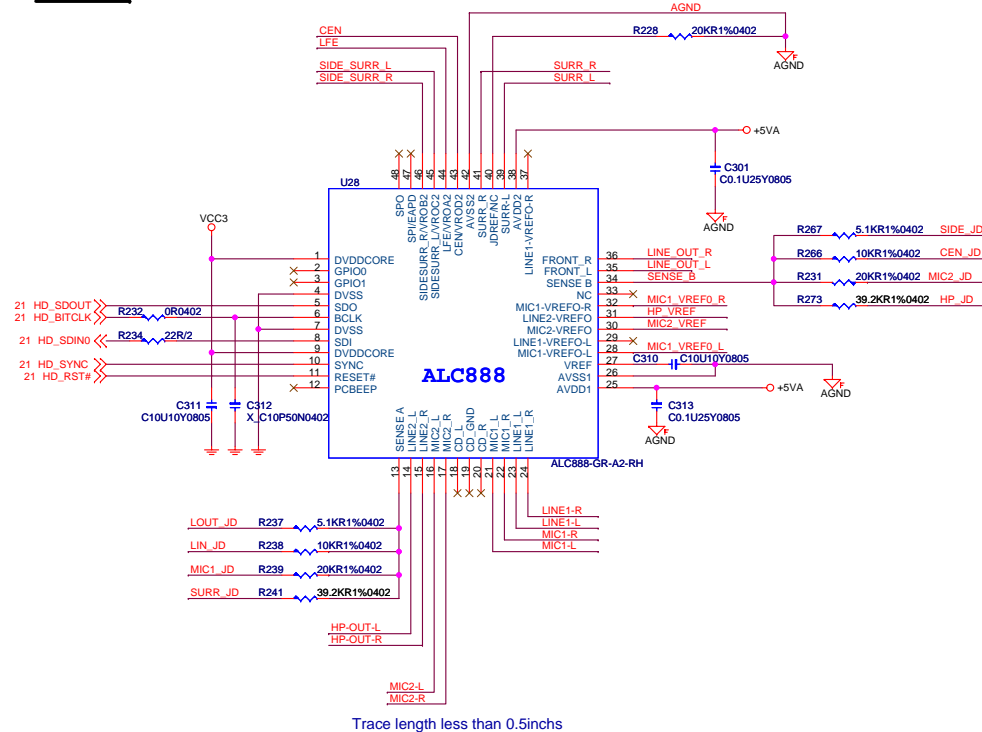
Internal reference  $V_{fb}=0.6V$  (+/- 1.5%,  
Better than external reference (+/-5%)  
==>Using Stand-alone mode



### DDR VTT Power



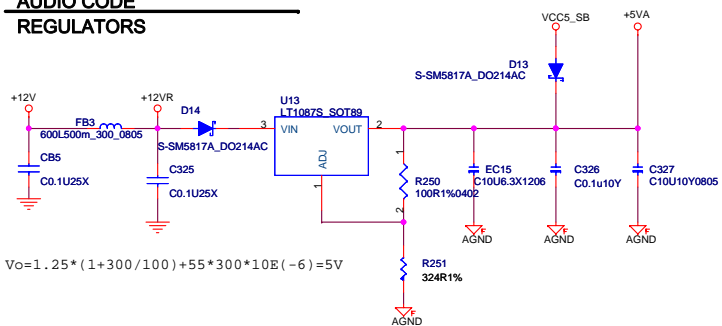
**ALC888**



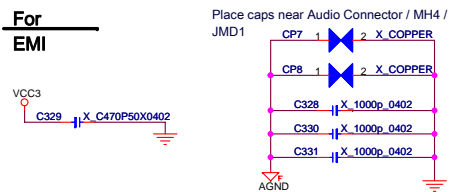
5.1 ch->N54-13F0171-S42  
R495&R496&R497&R498 =75  
Ohm,

7.1 ch-->N54-26F0111-K06  
R495&R496&R497&R498=1K  
Ohm

## AUDIO CODE REGULATORS

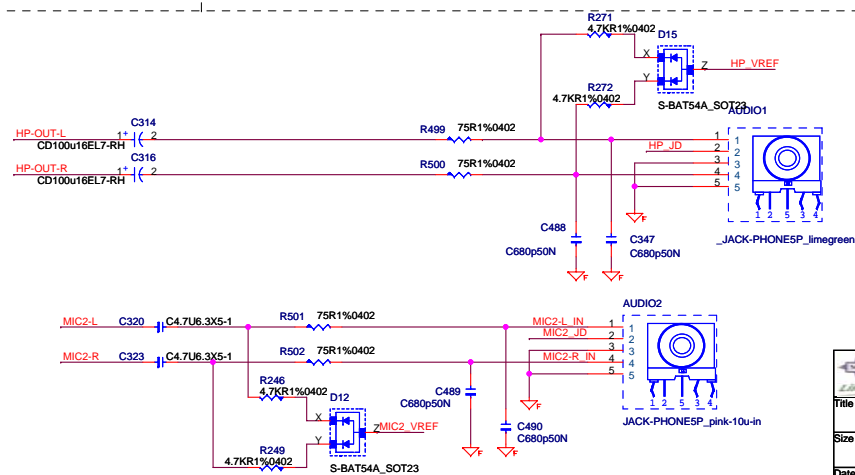
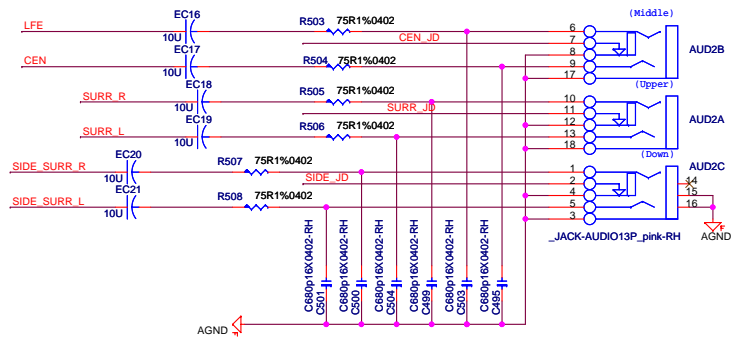
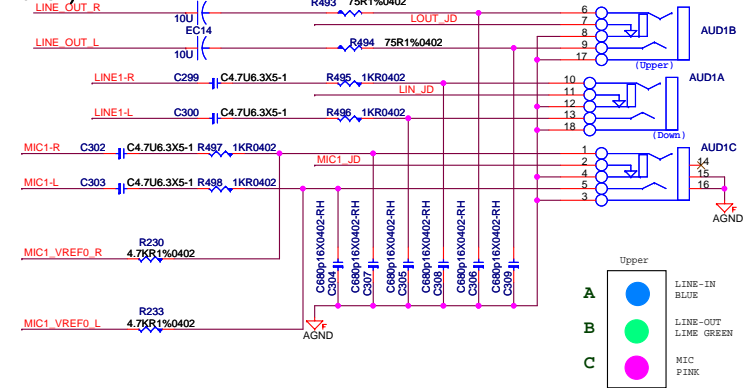



For  
EMI



PHONE JACKER (HDA

**JACK)**

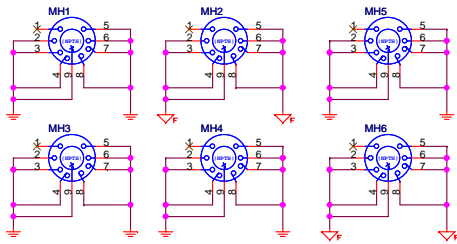


 <b>MSI</b> <i>Link to the Future</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <div style="text-align: center;"><b>AUDIO - ALC888</b></div>							
<b>Size</b>		<b>Document Number</b> <div style="text-align: center;"><b>MS-7445</b></div>				<b>Rev</b> <div style="text-align: center;"><b>0A</b></div>	
<b>Date:</b> Monday, December 23, 2008		<b>Sheet</b>		<b>28</b>		<b>of 32</b>	

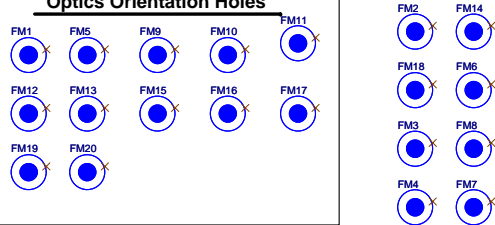


## Auto-BOM Manual Parts

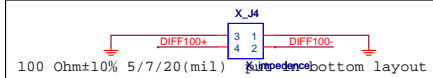
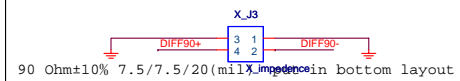
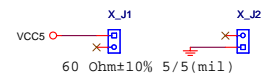
### Mounting Holes



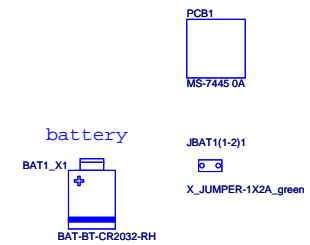
### Optics Orientation Holes



### Simulation



### MANUAL PART



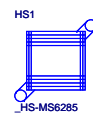
### CPU HEAT SINK



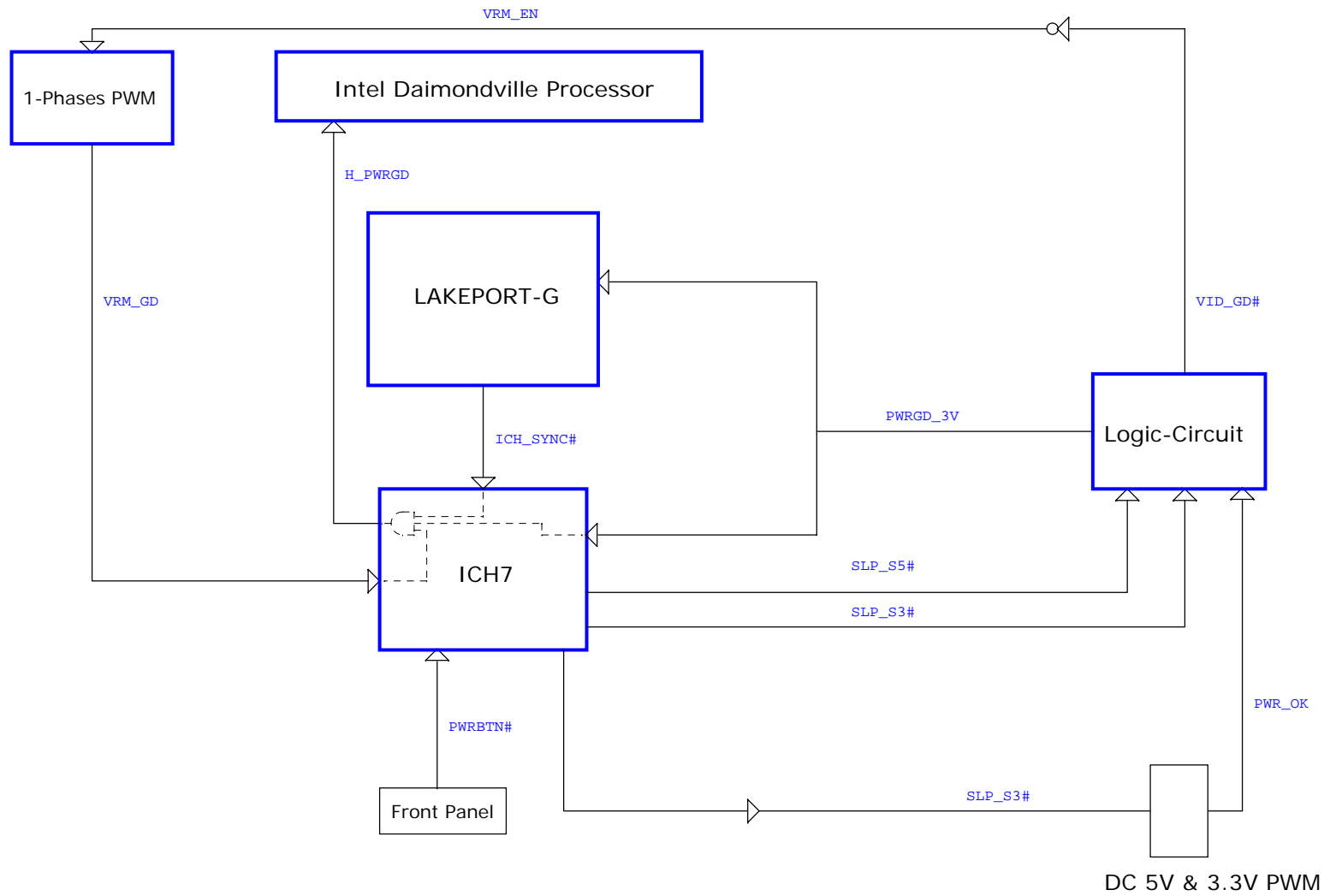
### NB HEAT SINK




### SB HEAT SINK




# PWROK MAP



 <b>MICRO-STAR INT'L CO., LTD.</b>	
Title PWOK MAP	
Size	Document Number MS-7445
Date: Friday, December 26, 2008	Rev 0A
Sheet 31 of 32	

1. Page 8 VID\_PG Refer to MS-96C4, VRM is enabled by FSB\_VTT
2. Page 8 VRM\_GD refer to MS-7440
3. Page 11 For DVI function, add DVI signals (reference from MS-7231)
4. Page 13 SO-DIMM slot change from N13-2000480-K06 to N13-2000190-A10
5. Page 15 MINI\_PCIE2 is stuffed
6. Page 16 change CLK GEN from ICS954119 to RTM876-665 (reference from MS-96C4)
7. Page 17 Add D17 to avoid leakage from monitor
8. Page 18 Add DVI chip- CH7307 reference from MS-7231
9. Page 21 change battery
10. Page 23 TPM unmount
11. Page 25 Power LED circuit modify, refer to MS-7440
12. Page 25 PSIN circuit modify, refer to MS-7440
13. Page 27 ACPI circuit modify
14. Page 30 Fan control circuit refer to MS-7440, control by SIO

		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title			
History			
Size	Document Number		Rev
	MS-7445		0A
Date:	Friday, December 26, 2008		Sheet 32 of 32